PRELIMINARY

YGV612

RPA2
Rendering Polygon Accelerator2

■ OVERVIEW

RPA2 is an LSI that processes 2D and 3D graphics on a PC at higher speeds.
Operations such as line drawing, Bit Blt, hidden surface removal by Z buffer, Gouraud shading and texture mapping can be performed by the hardware.
Combination of this LSI with a high speed MPU can configure high speed graphic systems. Since this LSI has a built-in DRAM controller, CRT controller and DAC, the configuration of the high speed system requires no external circuits except DRAMs and a clock generator. Then, the printed circuit board on which this LSI is mounted can be made smaller, resulting in reducing the number of components on the board, thus contributing to configuration of systems at lower cost.

■ FEATURES

- 2D/3D graphics
- Connects directly to PCI bus.
- 65536 colors with 16 bit color
- Up to 2048 × 1024 display space
- Hidden surface removal by 16 bit Z buffer
- Line drawing at 900 thousand vectors (10 pixels)/sec
- Bit Blt at 6.6 million pixels/sec.
- Polygon fill at 300 thousand polygons (50 pixel triangles, Gouraud shading)/sec
- Polygon fill at 150 thousand polygons (50 pixel triangles, Gouraud shading with texture)/sec
- Character transfer at 110 thousand characters (9 × 11)/sec
- Uses DRAM (64 kw × 16 b, 256 kw × 16 b) as a local memory.
- Available capacity of local memory : 512 kbytes, 1 Mbytes, 2 Mbytes or 4 Mbytes
- Has 16 b × 32 w command FIFO for host interface and 32 b × 8 w FIFO for reading or writing local memory.
- Has a programmable built-in display processor(CRT controller)
- Delivers linear RGB output using built-in DAC (Operating frequency up to 33 MHz)
- Interface for external RAMDAC (Operating frequency up to 70 MHz)
- Supports 8 bit general bus interface.
- Supports rectangular clipping.
- Operating frequency of master clock : up to 50 MHz
- +5 V power supply
- 208-pin QFP package

YAMAS024

● Commands and Functions

Command	>	Function
·Move_2D(X,Y)	>	Moves current position (CP) in two dimensional coordinate system.
·Draw_2D(X,Y)	>	Draws a line from CP to coordinate (X, Y).
·Move_3D(X,Y,Z,R,GB)	>	Moves CP in three dimensional coordinate system.
·Draw_3D(X,Y,Z,R,GB)	>	Draws a line from CP to coordinate (X, Y, Z) with shading.
·Triangle_Fill_2D(X,Y)	>	Fills triangular area with foreground color.
·Triangle_Fill_3D(X,Y,Z,R,GB)	>	Fills triangular area with Gouraud shading.
·BitBlt(Xsc,Ysc,Xs,Ys,Xe,Ye,)	>	Copies pixel data between rectangular areas.
·Rectangle_Fill(Xs,Ys,Xe,Ye)	>	Fills rectangular area with specified code.
·Pixel_Operation(Xs,Ys,Xe,Ye)	>	Transfers pixel data between CPU and local memories.
·Text_Operation(Xs,Ys,Xe,Ye)	>	Writes bit-map data into specified rectangular area using foreground or background color.
·Set_Linetype(P)	>	Defines bit pattern of up to 64 bits for drawing a line with a line type.
·Set_Linetype_Mode(SE)	>	Defines starting and ending locations within the bit pattern of 64 bits.
·Set_Texture_Offset(X,Y)	>	Defines rectangular area to be textured.
·Set_Texture_Size(Xs,Ys)	>	Selects one of 8 texture size types.
·Set_Texture_Triangle(X,Y)	>	Defines a texture that is pasted in triangular area.
·Set_Foreground_Color(AR,GB)	>	Defines foreground color.
·Set_Background_Color(AR,GB)	>	Defines background color.
·Set_Background_Z(Z)	>	Initializes rectangular area using predetermined value.
·Set_Logical_Operation(L)	>	Selects one of 16 logical operation types.
·Set_Bitplane_write_Mask(AR,GB)	>	Defines a bit plane where data write is inhibited.
·Set_Z_Offset(X,Y)	>	Defines area to be used as Z buffer.

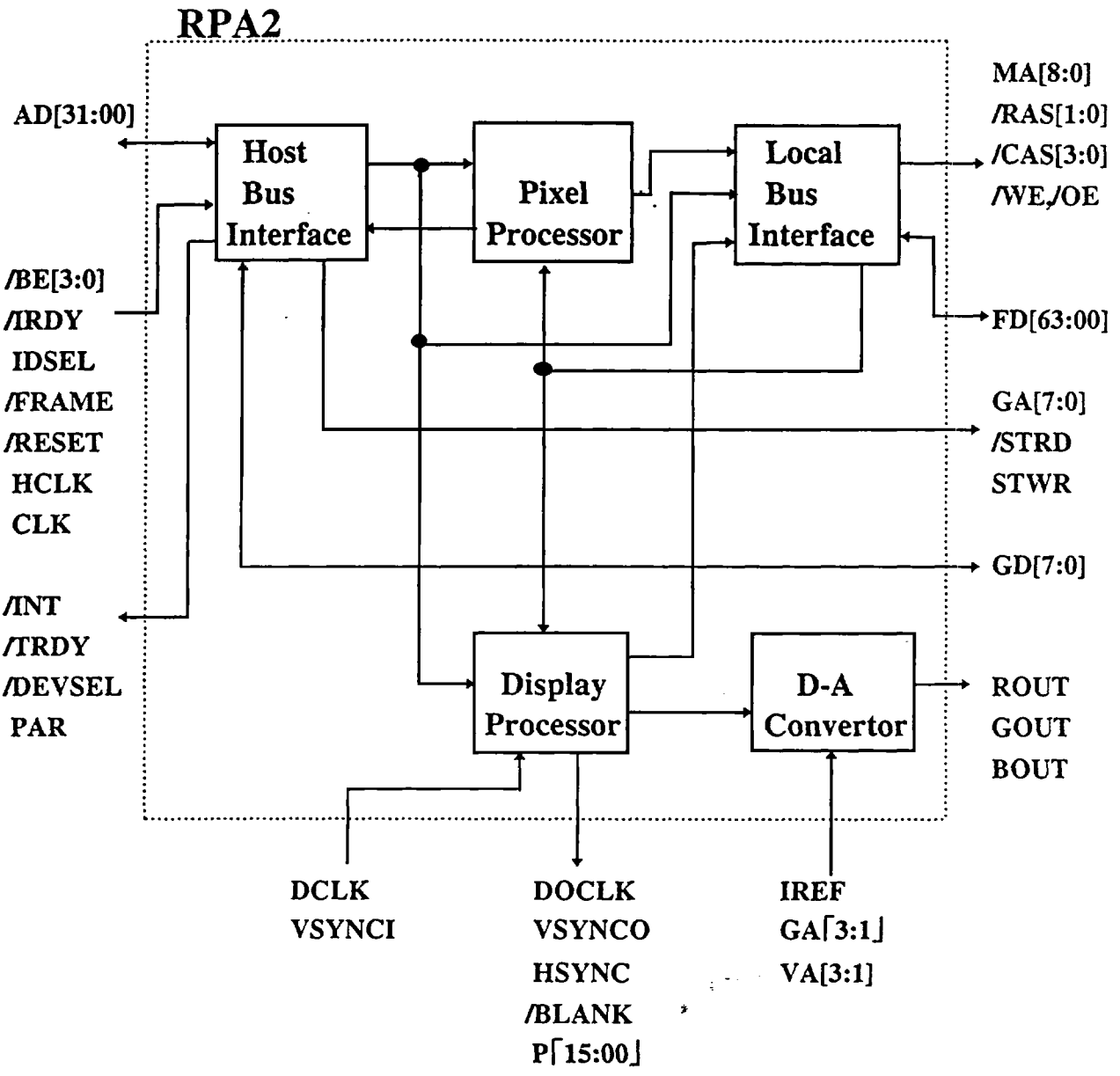
● **Memories to be used and Maximum Display Space**

512 kbytes	(Four 64 kw × 16 b DRAMs)	512 × 512
1 Mbytes	(Eight 64 kw × 16 b DRAMs)	1024 × 512
2 Mbytes	(Four 256 kw × 16 b DRAMs)	1024 × 1024
4 Mbytes	(Eight 256 kw × 16 b DRAMs)	2048 × 1024

● **Color Mode**

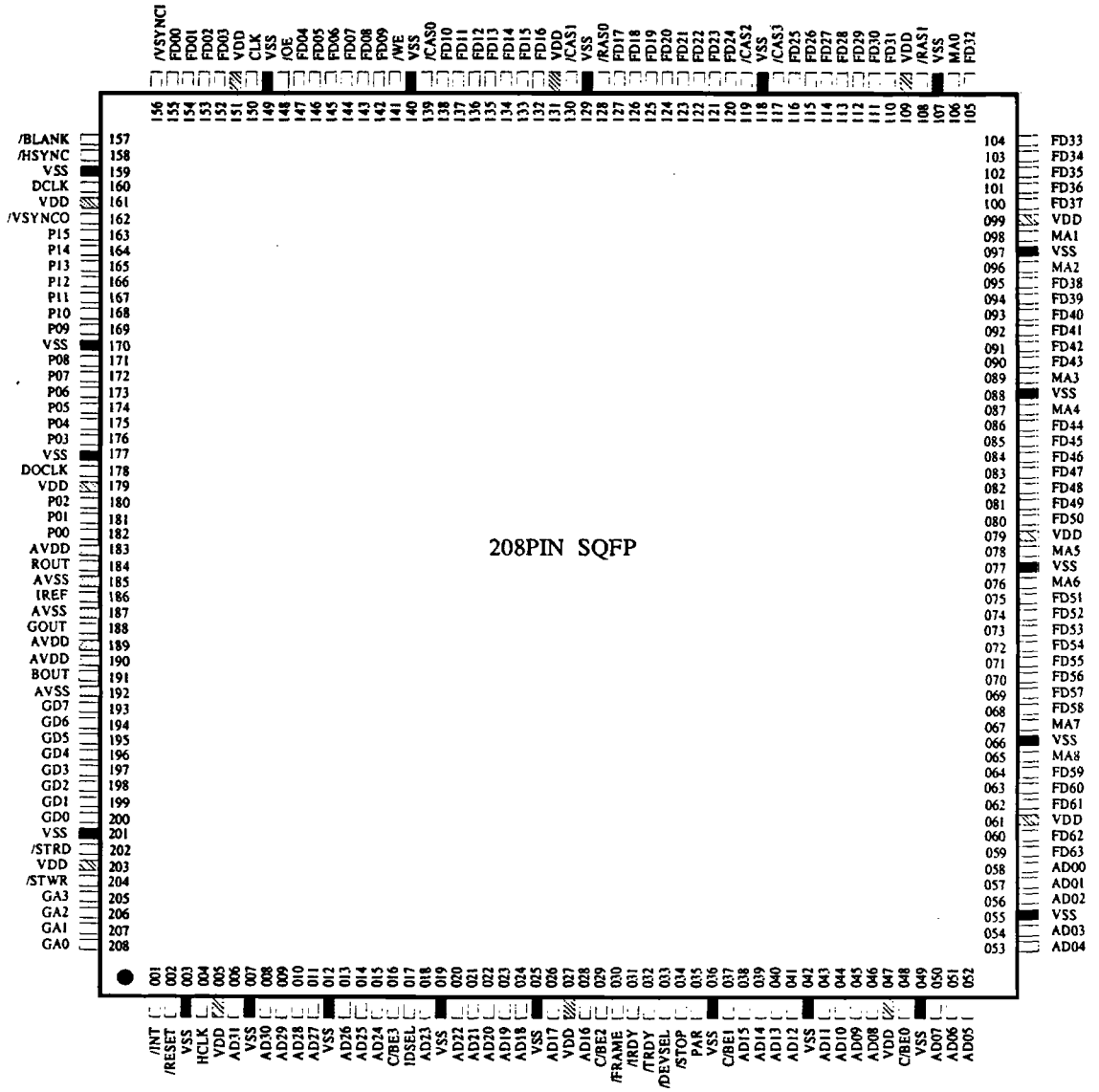
Color mode A = R6, G6, B4
Color mode B = R5, G6, B5
Color mode C = A1, R5, G5, B5 A : Attribute
Color mode D = A4, R4, G4, B4

■ BLOCK DIAGRAM



- ◆ **Host Bus Interface** = PCI, VL bus compatible interface
- ◆ **Pixel Processor** = Drawing processor
- ◆ **Local Bus Interface** = DRAM interface
- ◆ **Display Processor** = Display timing processor
- ◆ **D-A Convertor** = Digital to analog linear RGB converter

■ PIN CONFIGURATION DIAGRAM



■ FUNCTIONS OF PINS

● 1) Host Interface Pins

Signal Name (47 - pins)	Input/ Output	Description
AD[31:02]	I/O	Multiplexed address/data bus bits 31 : 02
AD01<57>	I/O	[PCI] Multiplexed address/data bus bit 01 [VL] Multiplexed memory I/O signal and data bit 1
AD00<58>	I/O	[PCI] Multiplexed address/data bus bit 00 [VL] Multiplexed read/write signal and data bit 0
C/BE[3:0] <16,29,37,48>	I	[PCI] Multiplexed bus command/byte enable signal 3:0 [VL] Byte enable signal 3:0
/IRDY<31>	I	[PCI] Initiator ready signal Indicates initiating agent's (bus master's) ability to complete current data phase of transaction. This signal is used in conjunction with /TRDY. [VL] Ready return signal
IDSEL<17>	I/O	[PCI] Initialization Device Selection signal Is used as a chip select during configuration read and write transactions. [VL] Data bus direction signal
/FRAME<30>	I	[PCI] Cycle frame signal Is driven by current master to indicate beginning and duration of an access. [VL] Address/data strobe signal
/RESET<2>	I	System reset
HCLK<4>	I	Host synchronous clock (max. 33 MHz)
CLK<150>	I	System clock (max. 50 MHz)
/INT<1>	O	Interrupt request signal to host. ※ At VL bus mode, Pull-up resistor of 1KΩ is externally required
/TRDY<32>	O	[PCI] Target ready signal Indicates target agent's (selected device's) ability to complete current data phase of transaction. [VL] Local ready signal
/DEVSEL<33>	O	[PCI] Device select signal When actively driven, this signal indicates that driving device has decoded its address as a target of current access. [VL] Local device signal
PAR<35>	O	[PCI] Parity signal Parity is even parity across AD[31::00] and C/BE[3::0]. [VL] Address bus enable signal
/STOP<34>	O	[PCI] Transaction stop request signal Indicates that current target is requesting master to stop current transaction. [VL] Data bus enable signal

● 2) Local Bus Interface

DRAMs up to 4 Mbytes is used as frame buffer, Z buffer or texture cache

Signal Name (81-pins)	Input/ Output	Description
FD [63:00]	I/O	Local memory data bus
MA [8:0]	O	Local memory address bus
/RAS [1:0]	O	Row address strobe signal
/CAS [3:0]	O	Column address strobe signal
/WE<141>	O	Write enable signal
/OE<148>	O	Data output enable signal

● 3) General Bus Interface

General Bus that can be interfaced to RAM DAC, ROM or any other device

Signal Name (14-pins)	Input/ Output	Description
GD [7:0]	I/O	General data bus
GA [3:0]	O	General address bus
/STRD <202>	O	Read strobe signal
/STWR <204>	O	Write strobe signal

● 4) Display Interface

Transfers data, timing signal and output of built-in DAC to RAMDAC.

Signal Name (32-pins)	Input/ Output	Description
/VSYNCI <156>	I	Vertical Sync signal input
/VSYNCO <162>	O	Vertical Sync signal output
DCLK <160>	I	Display dot clock input (max. 70 MHz)
DOCLK <178>	O	Display dot clock output
/HSYNC <158>	O	Horizontal Sync signal output
/BLANK <157>	O	Display blank signal output
P [15 : 00]	O	Video data to RAM DAC: A color mode is selected from [R6.G6.B4], [R5.G6.B5], [A1.R5.G5.B5] or [R4.G4.B4.A4] and specified in the order as [P15---P00].
ROUT <184>	O	Analog red signal
GOUT <188>	O	Analog green signal
BOUT <191>	O	Analog blue signal
IREF <186>	I	Internal DAC reference current
AVSS <185>	I	Analog ground 1
AVSS <187>	I	Analog ground 2
AVSS <192>	I	Analog ground 3
AVDD <183>	I	Analog power supply 1
AVDD <189>	I	Analog power supply 2
AVDD <190>	I	Analog power supply 3

■ HOST INTERFACE

● 1) Address Map

Host CPU transfers data with RPA2 through host interface.

AD12	AD11	AD[10:02]	Read/Write	Within 1 Mbyte boundary
AD24	AD23	AD[22:02]	Read/Write	Outside 1 Mbyte boundary
L	L	Don't Care	Read	reserved
L	L	Don't Care	Write	Index register
L	H	Don't Care	Read	Status register
L	H	Don't Care	Write	Control register
H	L	Don't Care	Read	reserved
H	L	Don't Care	Write	Command FIFO register
H	H	Don't Care	Read	Memory read FIFO register
H	H	Don't Care	Write	Memory write FIFO register

● 2) I/O Map

Host CPU is able to select memory map or I/O map.

AD03	AD02	Read/Write	Name of register
L	L	Read	reserved
L	L	Write	Index register
L	H	Read	Status register
L	H	Write	Control register
H	L	Read	reserved
H	L	Write	Command FIFO register
H	H	Read	Memory read FIFO register
H	H	Write	Memory write FIFO register

● 3) Index Register

RPA2 includes 19 control registers, two status register and 16 general bus space registers.

Index register specifies a register to be accessed.

MSB LSB

0	0	0	0	0	0	0	0	0	0	RA5	RA4	RA3	RA2	RA1	RA0

● 4) Status register

In status register, either of two types of flag registers or a general bus is readable.

	RA4	RA3	RA2	RA1	RA0	Read Only Register
L	L	L	L	L	L	System flag register
L	L	L	L	L	H	FIFO flag register
H	L	GA3	GA2	GA1	GA0	General bus register(Address is set with GA3 to GA0.)

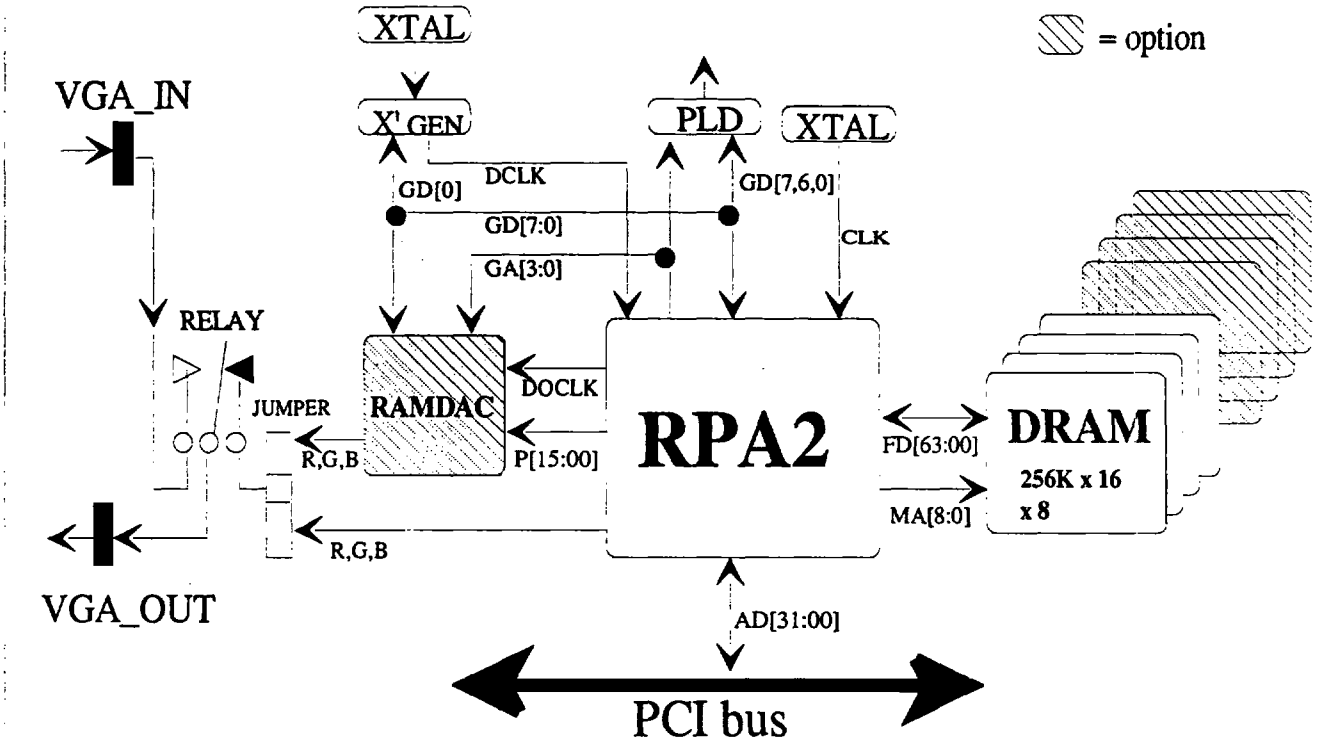
※ Any setting other than the above is ineffective.

● 5) Control Register

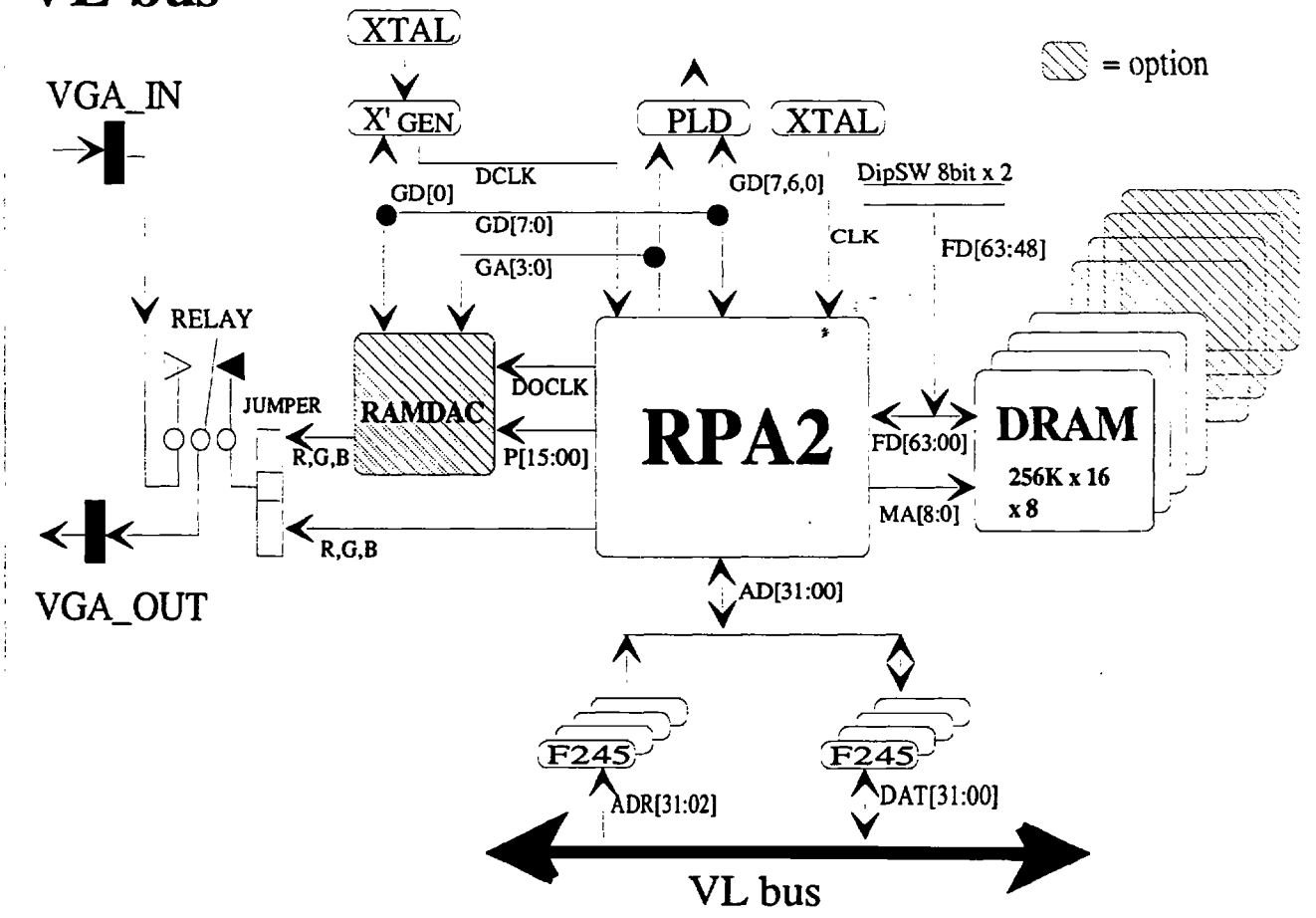
RA5	RA4	RA3	RA2	RA1	RA0	Write Only Register
L	L	L	L	L	L	System register
L	L	L	L	L	H	Configuration register
L	L	L	L	H	L	Vertical Sync cycle register
L	L	L	L	H	H	Vertical Sync signal width register
L	L	L	H	L	L	Vertical Sync blank falling edge register
L	L	L	H	L	H	Vertical Sync blank rising edge register
L	L	L	H	H	L	Horizontal Sync cycle register
L	L	L	H	H	H	Horizontal Sync signal width register
L	L	H	L	L	L	Horizontal Sync blank falling edge register
L	L	H	L	L	H	Horizontal Sync blank rising edge register
L	L	H	L	H	L	Display start X address register
L	L	H	L	H	H	Display start Y address register
L	L	H	H	L	L	reserved
L	L	H	H	L	H	reserved
L	L	H	H	H	L	Display control register
L	L	H	H	H	H	reserved
L	H	L	L	L	L	Vertical Blank flags count register
L	H	L	L	L	H	General Bus Control register
L	H	L	L	H	L	reserved
L	H	L	L	H	H	reserved
L	H	L	H	L	L	Clipping Boundary Left register
L	H	L	H	L	H	Clipping Boundary Right register
L	H	L	H	H	L	Clipping Boundary Top register
L	H	L	H	H	H	Clipping Boundary Bottom register
L	H	H	x	x	x	reserved
H	L	GA3	GA2	GA1	GA0	Write data to General Bus register (Address is set with GA3 to GA0.)
H	H	x	x	x	x	reserved

EXAMPLE OF SYSTEM CONFIGURATION

PCI bus



VL bus



■ Electrical Characteristics ['95/08/24]

● Absolute Maximum Ratings

Power supply voltage	-0.3 to 7.0 V
Input voltage	-0.3 to VDD+0.5 V
Operating temperature	0 to 70 ℃
Storage temperature	-50 to 125 ℃

● Recommended Operating Condition

	Symbol	Min	Typ	Max	Unit
Power supply voltage		4.75		5.25	V
IREF current		3.5		5.5	mA
Operating temperature		0		70	℃

● Digital DC Characteristics

	Symbol	Min	Typ	Max	Unit
Power supply current *1	IDD			250	mA
Input high voltage	VIH	2.2			V
Input low voltage *2	VIL			0.8	V
Input low voltage *3	VIL			0.5	V
Output high voltage *4	VOH	2.4			V
Output low voltage *4	VOL			0.4	V
Input leak current	IL			10	uA
Input capacitance	CI			10	pF
Output tri-state leak	IZ			10	uA
Output capacitance	CO			10	pF

*1 at the condition of VDD=5V,DAC active,CLK=50MHz,HCLK=33MHz,DCLK=25MHz

*2 for pins except FD[63:00]

*3 for pins FD[63:00]

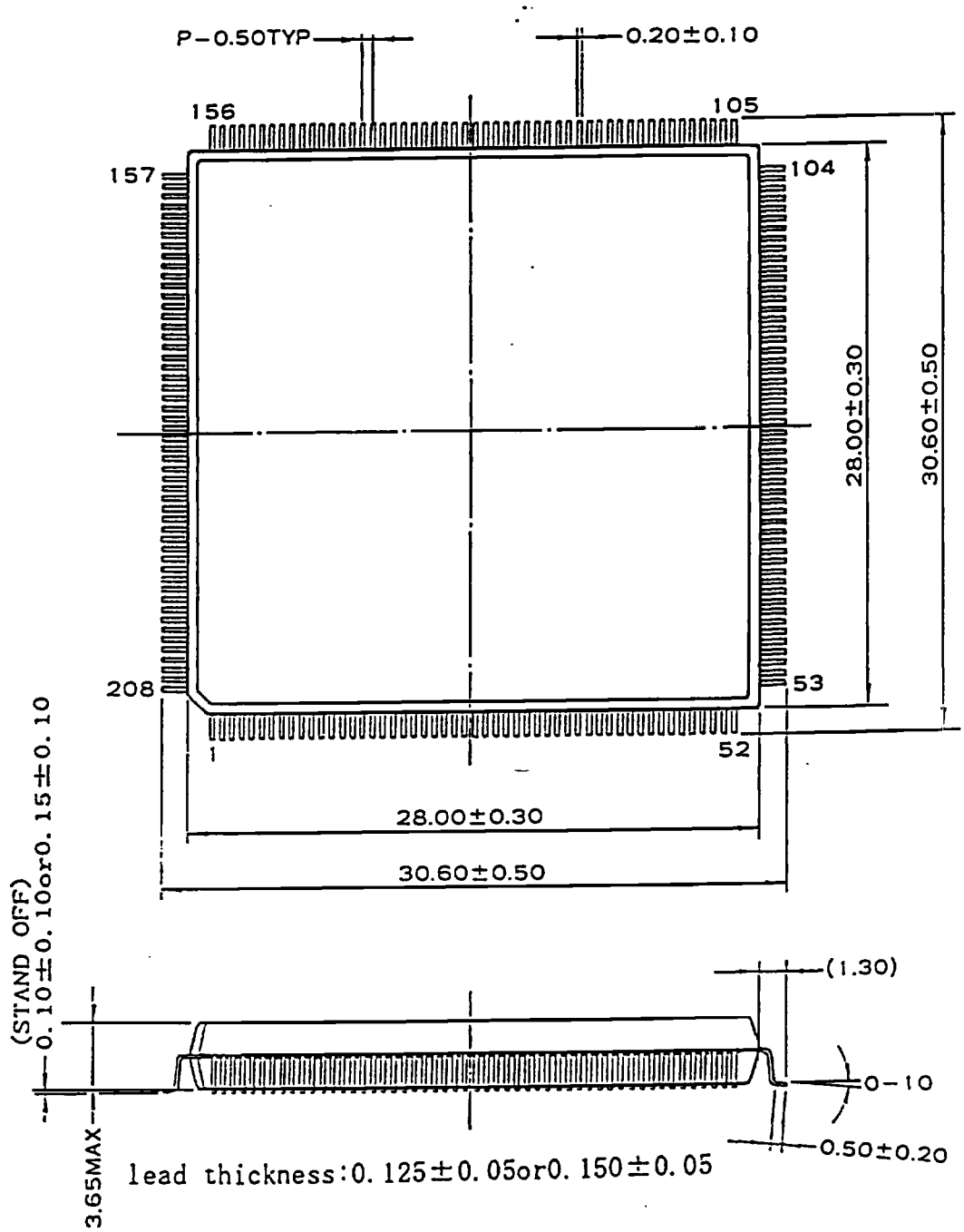
*4 IOH=8mA,IOL=8mA for /INT,AD[31:00],IDSEL,/TRDY,/DEVSEL,/STOP,PAR
IOH=4mA,IOL=4mA for /VSYNCO,/BLANK,/HSYNC,DOCLK,P[15:00],
MA[8:0],/RAS[1:0],/CAS[3:0],/WE,/OE
IOH=2mA,IOL=2mA for FD[63:00],GD[7:0],GA[3:0],/STRD,/STWR

● DAC DC Characteristics

	Min	Typ	Max	Unit
Resolution		6		bit
Integral linearity error			±1	LSB
Differential linearity error			±1	LSB
Output full scale current factor N *1	4.0	5.1	5.8	

*1 Iout=IREF*N at ROUT=37.5Ω

■ EXTERNAL DIMENSIONS



The dimension in parentheses is for referemce only.
The mold external dimensions do not include flash.
UNIT: mm

NOTE: The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

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AGENCY

YAMAHA CORPORATION

Address inquiries to :
Semi-conductor Sales Department

■ Head Office 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-01
Electronic Equipment business section
Tel. 0539-62-4918 Fax. 0539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku, Tokyo, 108
Tel. 03-5488-5431 Fax. 03-5488-5088

■ Osaka Office 3-12-9, Minami Senba, Chuo-ku, Osaka City, Osaka, 542
Shinsaibashi Plaza Bldg. 4F
Tel. 06-252-7980 Fax. 06-252-5615

■ U.S.A. Office YAMAHA Systems Technology,
100 Century Center Court, San Jose, CA 95112
Tel. 408-467-2300 Fax. 408-437-8791

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